

REMARKS

As a preliminary matter, Applicants appreciate the Examiner's allowance of claim 17.

Claims 14 and 18-19 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Koike et al. (U.S. Patent No. 5,781,253) in view of Fujita et al. (U.S. Patent No. 6,184,966). In response, Applicants amended independent claim 14 to clarify that the resistive component having a resistance of 7 to 8 k Ω is formed between the metal layer and the connecting layer.

Koike is directed to a liquid crystal display having electrostatic discharge protection and method for manufacturing the same. In FIGs. 2-3, the Examiner asserts that discharge projections 52, 54 correspond to a plurality of metal layers, and metal wiring layer 48 corresponds to a connecting layer of the present invention. However, Koike fails to disclose or suggest a resistive component having a resistance of 7 to 8 k Ω being formed between the metal layers and the connecting layer, as now recited in the amended claims. Fujita also fails to disclose or suggest this feature.

In contrast, as discussed in Applicants' specification on page 47, line 26 to page 48, line 1, when Ti is used for a lower layer metal, a heat treatment is performed before depositing the indium tin oxide (ITO). Therefore, when a diameter of a contact hole 98 is 4 μ m, a resistive component can be formed as 7 to 8 k Ω . Since Koike and Fujita fail to disclose or suggest this feature, withdrawal of the §103(a) rejection of claims 14 and 18-19 is respectfully requested.

Claim 15 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al. (U.S. Patent No. 6,043,971) in view of Matsumoto (U.S. Patent No. 6,211,534). In response, Applicants amended claim 15 like claim 14, and respectfully traverse the rejection for the same reasons recited above with respect to the rejection of claim 14.

Song is directed to an electrostatic discharge protection device for a liquid crystal display using a chip on glass package. As correctly noted by the Examiner, Song fails to disclose the structure of an electrostatic protection element portion. However, the Examiner cites Matsumoto as teaching this feature.

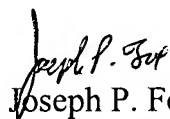
Matsumoto is directed to a thin film transistor array and method for fabricating the same. In FIGs. 2-4 of Matsumoto, the Examiner identifies a plurality of metal layers as corresponding to elements 4 and 7. A connecting layer is identified as the coupling conductor portion 27a, and the connecting layer is considered to electrically connect the metal layers via the contact hole. However, Matsumoto is silent regarding a resistive component being formed between the metal layers and the connecting layer that has a resistance of 7 to 8 k Ω . Accordingly, withdrawal of the §103(a) rejection of claim 15 is respectfully requested.

For all of the foregoing reasons, Applicants submit that this Application is in condition for allowance, which is respectfully requested. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

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